MN3102

CMOS CLOCK GENERATOR/DRIVER FOR LOW VOLTAGE OPERATION BBD

■ General description

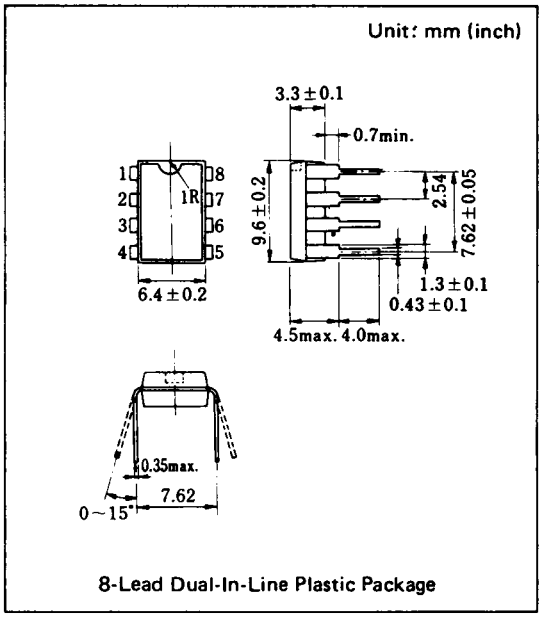
The MN3102 is a CMOS LSI generating two phase clock signal of low output impedance necessary to drive MN3200 series low voltage operation BBD.

V_{GG} power supply circuit is built-in exclusively used for the MN3200 series BBD* and most suitable V_{GG} voltage can be obtained when the MN3102 is used with the same supply voltage as BBD.

Self-oscillation is enabled by external capacitors and resistors and oscillation drive is possible by the separate excitation oscillation.

Clock signal frequency is 1/2 of oscillation freguency.

* MN3200 Series BBD
MN3204, MN3205, MN3206, MN3207, MN3208, MN3209, N3210 MN3214.

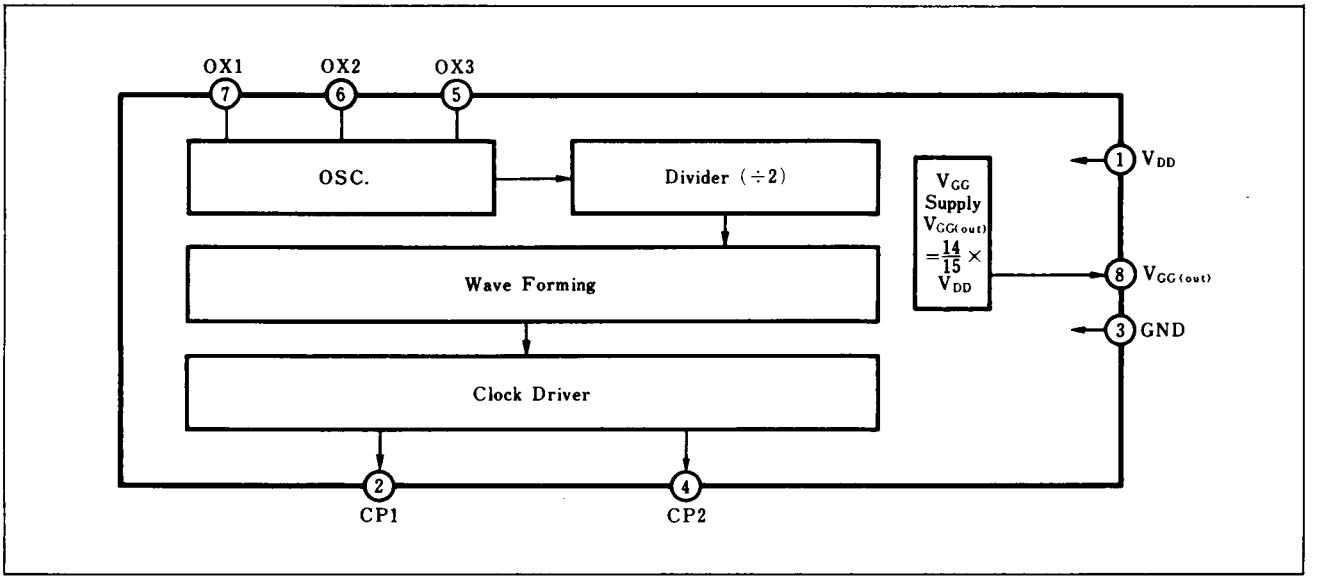


8-Lead Dual-In-Line Plastic Package

■ Features

- Direct driving capability to 4096-stage low voltage BBD.
- Self oscillation and separate exitation are abled.
- Two phase clock (Duty: 1/2) output.
- V_{GG} voltage generator for low voltage BBD.
- Single supply source: 4 ~ 10V.
- 8-lead dual-in-line plastic package.

■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain Supply Voltage	V_{DD}	−0.3~+12	V
Input Output Terminal Voltage	V_I, V_O	−0.3~V_{DD}+0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature	Topr	−10~+70	℃
Storage Temperature	Tstg	−30~+125	℃

■ Operating Condition (Ta = 25°C)

Item	Symbol	Condtion	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	GND=0V	4	5	10	V

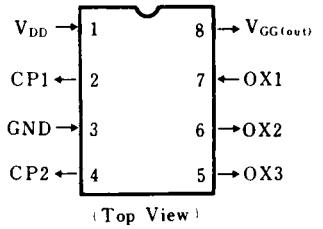
■ Electrical Characteristics (Ta = 25°C, V_{DD} = 5V, GND = 0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Current	I_{DD}	No load		0.5		mA
Total Power Dissipation	P_{tot}	Clock output 40kHz		2.5		mW
OX1 Input Terminal						
Input Voltage "H" Level	V_{IH}		V_{DD}−1		V_{DD}	V
Input Voltage "L" Level	V_{IL}		0		1	V
Input Leakage Current	I_{Leak}	V_I=0~10V			30	μA
OX2 Output Terminal						
Output Current "H" Level	$I_{OH(1)}$	V_{DD}=5V, V_O=4V	0.5			mA
Output Current "L" Level	$I_{OL(1)}$	V_{DD}=5V, V_O=1V	0.4			mA
Output Leakage Current "L" Level	$I_{LOL(1)}$	V_{DD}=10V, V_O=GND			30	μA
Output Leakage Current "H" Level	$I_{LOH(1)}$	V_{DD}=10V, V_O=V_{DD}			30	μA
OX3 Output Terminal						
Output Current "H" Level	$I_{OH(2)}$	V_{DD}=5V, V_O=4V	0.7			mA
Output Current "L" Level	$I_{OL(2)}$	V_{DD}=5V, V_O=1V	1			mA
Output Leakage Current "L" Level	$I_{LOL(2)}$	V_{DD}=10V, V_O=GND			30	μA
Output Leakage Current "H" Level	$I_{LOH(2)}$	V_{DD}=10V			30	μA
CP1, CP2 Output Terminal						
Output Current "H" Level	$I_{OH(3)}$	V_{DD}=5V, V_O=4V	5			mA
Output Current "L" Level	$I_{OL(3)}$	V_{DD}=5V, V_O=1V	5			mA
Output Leakage Current "L" Level	$I_{LOL(3)}$	V_{DD}=10V, V_O=GND			30	μA
Output Leakage Current "H" Level	$I_{LOH(3)}$	V_{DD}=10V, V_O=V_{DD}			30	μA
$V_{GG\ (OUT)}$ Output Terminal						
V_{GG} Output Voltage *1	$V_{GG(OUT)}$			4.67		V

*1 This terminal generates V_{GG} voltage exclusively applied for low voltage operation BBD manufactured by Matsushita Electronics Corporation, Therefore, sometimes it might not applicable for the device other than V_{GG} voltage of low power operation of BBD by MEC. $V_{GG\ (OUT)}$ changes in the following formula depending on the value of V_{DD}.

$$V_{GG\ (OUT)} = 14/15\ V_{DD}$$

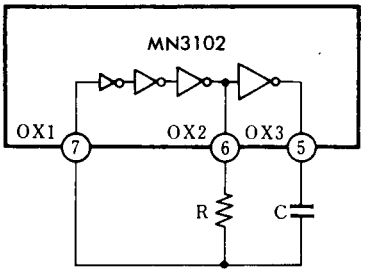
■ Terminal Assignments



■ Terminal Description

Terminal No.	Symbol	I/O	Terminal Name	Description	
1	V_{DD}	Power supply source	V_{DD} is applied	Supply voltage of 4 ~ 10 is applied.	
2	CP1	0	Clock output 1	The terminal outputs clock signal with the relation of reverse phase to CP2, which is a frequency with duty 1/2 and 1/2 of the oscillation frequency.	
3	GND	Power supply source	Earth	Connected to the earth of circuit.	
4	CP2	0	Clock output 2	Outputs clock signal with the reverse phase to CP1.	
5	OX3	0	C and R are connected.	In case of self-oscillation, C and R are connected. (Refer to the example of oscillation circuit).	In case of separate excitation oscillation, OX3 and OX2 should be opened. OX1 is set to OSC input.
6	OX2	0			
7	OX1	1			
8	$V_{GG\ (OUT)}$	0	V_{GG} voltage output.	4.67V is output. (V_{DD} = 5V). $V_{GG\ (OUT)} = 14/15V_{DD}$	

■ Example of Oscillation Circuit



Oscillation circuit of the MN3102 is composed of 4-stage inverter and oscillation frequency is defined by the C, R time constant.

Following is an example of C, R. Figure 1 shows fcp*—R characteristics.

Example \ Constant	R (Ω)	C (pF)	f_{OSC}** (kHz)	f_{CP}* (kHz)
Example (1)	5k~1M	22	20 ~1400	10 ~700
Example (2)	5k~1M	100	6.4~ 520	3.2~260
Example (3)	5k~1M	200	3.0~ 260	1.5~130

* Clock output frequency of CP1 or CP2 terminals.
** Oscillation frequency of OX1, OX2 and OX3.

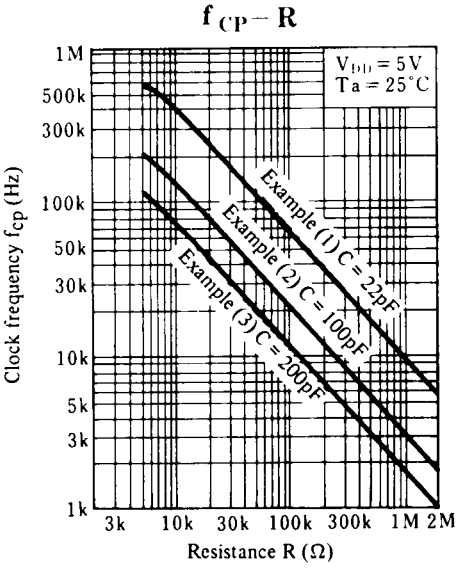


Figure 1 Example of Clock Oscillation Frequency Characteristics

■ The maximum clock fraquency

The upper limit of the value of clock frequency is determined depending on the load capacitance and power consumption.
The permissible dissipation for this LSI is: P_D = 200mW.
If the lock frequency or the load capacitance is increased, the power consumption will be increased. (Refer to Figure 2.) Accordingly, in order to use the MN3102 with dissipation less than the permissible value, it is necessary to select adequate values for the clock frequancy and load capacitance.
Figure 3 shows an example of the dependence of the maximum clock frequency in P_D = 200mW on the load capacitance. If V_{DD} is less than 7V, the dissipation will not exceed the permissible value. (Provided that the BBD equivalent to less than 4096 steps in used.)

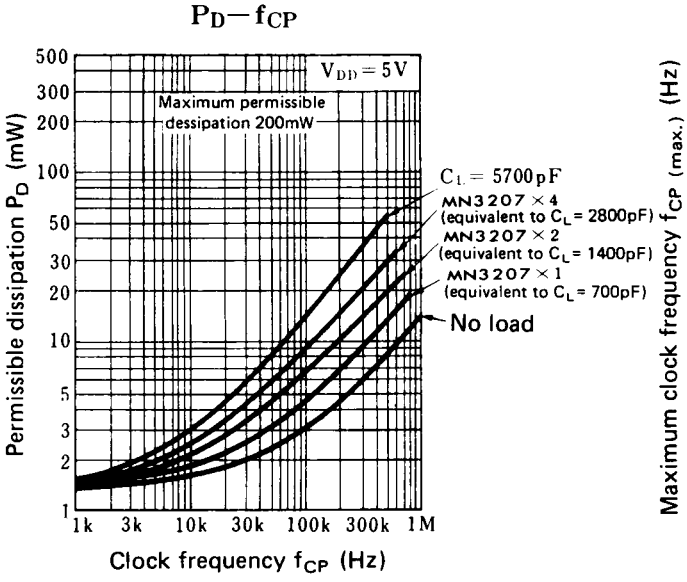


Figure 2 Example of the dependence of power consumption on the clock frequency.

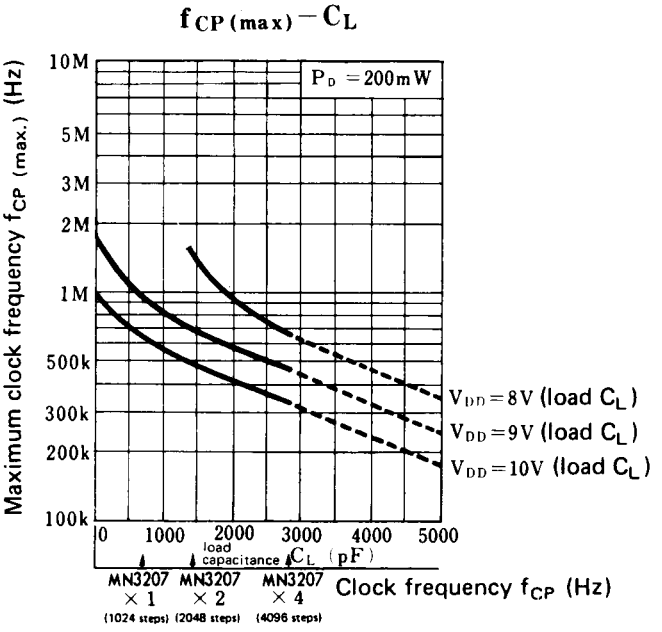


Figure 3 Example of the dependence of the maximum clock frequency on the load capacitance in the power consumption of 200mW.