ELFA artikelnr.

73-774-43 DS1869-10 **73-774-50 DS1869S-10**

DALLAS SEMICONDUCTOR

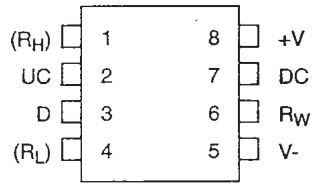
DS1869

3V Dallastat™ Electronic Digital Rheostat

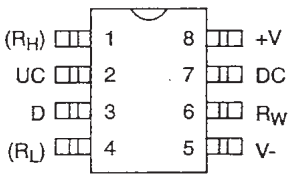
FEATURES

- Replaces mechanical variable resistors
- Operates from 3V or 5V supplies
- Electronic interface provided for digital as well as manual control
- Wiper position is maintained in the absence of power
- Low cost alternative to mechanical controls
- Applications include volume, tone, contrast, brightness, and dimmer control
- 8–pin SOIC and 8–pin DIP packages for DS1869
- Standard resistance values for Dallastat
  - DS1869–10 ~ 10KΩ
  - DS1869–50 ~ 50KΩ
  - DS1869–100 ~ 100KΩ
- Operating Temperature Range
  - Commercial: 20°C to 70°C
- 3V to 8V differential supplies operational range

PIN ASSIGNMENT



8-Pin DIP (300 Mil)
See Mech. Drawings Section



8-Pin SOIC (208 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

R_H	-	Resistor High End (Option)
R_W	-	Resistor Wiper
R_L	-	Resistor Low End
-V, +V	-	Voltage Inputs
UC	-	Up Contact Input
D	-	Digital Input
DC	-	Down Contact Input

DESCRIPTION

The DS1869 Dallastat is a digital rheostat or potentiometer. This device provides 64 possible uniform tap points over the resistive range and is available in standard versions of 10K, 50K, and 100K ohms. The Dallastats can be controlled by either a mechanical–type contact closure input or a digital source input such as a CPU, and the DS1869 operates from 3V or 5V supplies. Wiper position is maintained in the absence of power which is accomplished through the use of a EEPROM memory cell array. The EEPROM cell array is specified to accept greater than 50,000 writes.

The DS1869 is offered in two standard IC packages which include an 8–pin 300 mil DIP and an 8–pin 200 mil SOIC. The DS1869 can be configured to operate using a single pushbutton, dual pushbutton or digital source input. This is illustrated in Figure 1. The DS1869 pinouts allow access to both ends of the potentiometer RL, RH, and the wiper, RW. Control inputs include the digital source input, D, the up contact input, UC, and the down contact input, DC. Other pins include the positive,+V, and negative, –V , supply inputs. The DS1869 is available in commercial temperature versions.

OPERATION

The DS1869 can be configured to operate from a single contact closure, dual contact closure inputs or driven using a digital source input. Figures 1 and 2 illustrate both configurations, respectively. Contact closure is defined as the transition from a high level to a low level on the up contact (UC), down contact (DC), or digital source (D) inputs. These inputs are inactive when in the high state.

The DS1869 interprets input pulse widths as the means of controlling wiper movement. A single pulse input over the UC, DC, or D input terminals will cause the wiper position to move 1/64th of the total resistance. A transition from a high to low on these inputs is considered the beginning of pulse activity or contact closure. A single pulse is defined as being greater than 1 ms but lasting no longer than 1 second. This is shown is Figures 3, 4, and 5 (a).

Repetitive pulsed inputs can be used to step through each resistive position of the device in a relatively fast manner (see Figure 5b). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the DS1869 will interpret repetitive pulses as a single pulse.

Pulse inputs lasting longer 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given by the formula below:

$$\approx 1 \text{ second} + 63 \times 100 \text{ ms} = 7.3 \text{ (seconds)}$$

Single contact closure operation allows the user to control wiper movement in either direction from a single push–button input. Figure 1 presents a typical single push–button configuration. The UC input is used to increment and decrement wiper position for single push–button mode of operation. The DC input provides no functionality in this mode but must be connected to the positive supply voltage (V_{CC}). The digital source input (D) can be allowed to float.

On device power–up, the configuration shown in Figure 1 must exist in order to enter the single contact closure mode of operation; especially and specifically, the (DC) input's connection to the positive supply voltage (V_{CC}) .

The direction of wiper movement, in single push–button operation, is determined by prior activity; with the direction of wiper movement being opposite to that of the previous activity.

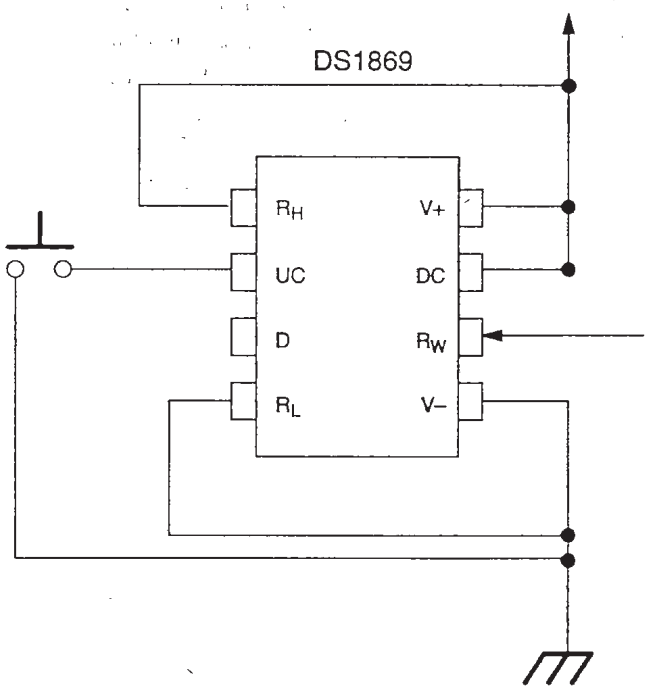
Changing the direction of wiper movement in single push–button mode is accomplish by a period of inactivity on the UC input of a (minimum) 1 second or greater. Also, in single push–button mode, as the wiper reaches the end of the potentiometer range its direction of movement reverses. This will occur, regardless, if the input is a continuous pulse, a sequence of repetitive pulses or a single pulse.

Dual push–button mode of operation is accomplished when the DC input is floated on power–up. If interfacing contact closure control inputs to digital logic, the DC input must be interfaced to an open drain drive which is high impedance during power–up. This will prevent the device from entering a single push–button mode of operation.

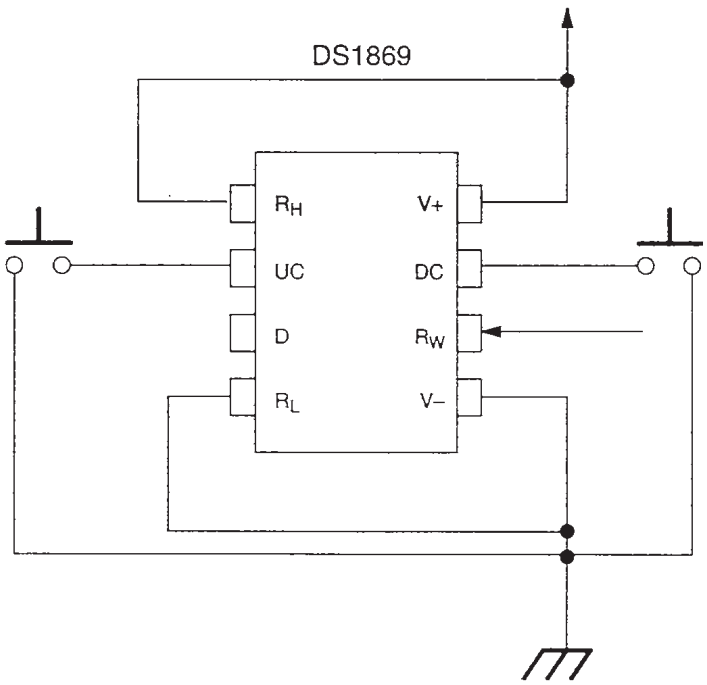
In dual push–button mode, each direction is controlled by the up contact (UC) and down contact (DC) inputs, respectively. No wait states are required to change wiper direction in dual push–button mode. In dual push–button mode, as the wiper position reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All contact closure control inputs, UC, DC, and D are internally pulled–up by a 100K ohm resistance. The UC and DC inputs are internally debounced and require no external components for input signal conditioning.

DS1869 SINGLE PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 1



DS1869 DUAL PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 2



The DS1869 is provided with two supply inputs –V and +V. The maximum voltage difference between the two supply inputs is + 8.0 volts while the minimum voltage difference is 2.7 volts. All input levels are referenced to the negative supply input, –V. The voltage applied to any Dallastat terminal must not exceed the negative supply voltage (–V) by –0.5 or the positive supply voltage (+V) by + 0.5 volts. The minimum logic high level must be +2.4 volts with reference to the –V supply voltage input for +V=5V. A logic low level with reference to the –V supply voltage has a maximum value of +0.8 volts. Dallastats exhibit a typical wiper resistance of 400 ohms with a maximum wiper resistance of 1000 ohms. The maximum wiper current allowed through the Dallastat is specified at 1 milliamps (see DC Electrical Characteristics).

NONVOLATILE WIPER SETTINGS

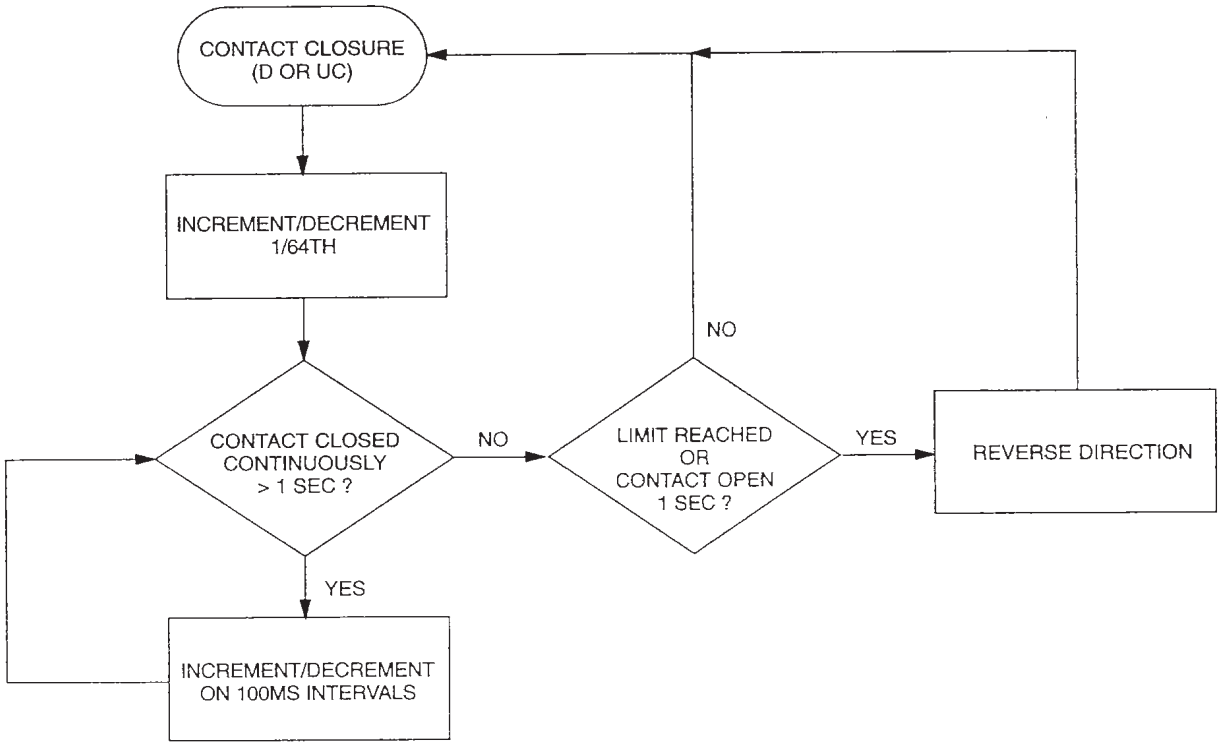
Dallastats maintain the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation the position of the wiper is determined by the input multiplexer. Periodically, the multiplexer will update the EEPROM memory cells. The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the Dallastat, the wiper setting will be the last recorded in the EEPROM memory cells. If the Dallastat setting is changed after power is applied, the new value will be stored after a delay of 2 seconds. The initial storage of a new value after power–up occurs when the first change is made, regardless of when this change is made.

After the initial change on power–up, subsequent changes in the Dallastat EEPROM memory cells will occur only if the wiper position of the part is moved greater than 12.5% of the total resistance range. Any wiper movement after initial power–up which is less than 12.5% will not be recorded in the EEPROM memory cells. Since the Dallastat contains a 64–to–1 multiplexer, a change of greater than 12.5% corresponds to a change of the fourth LSB.

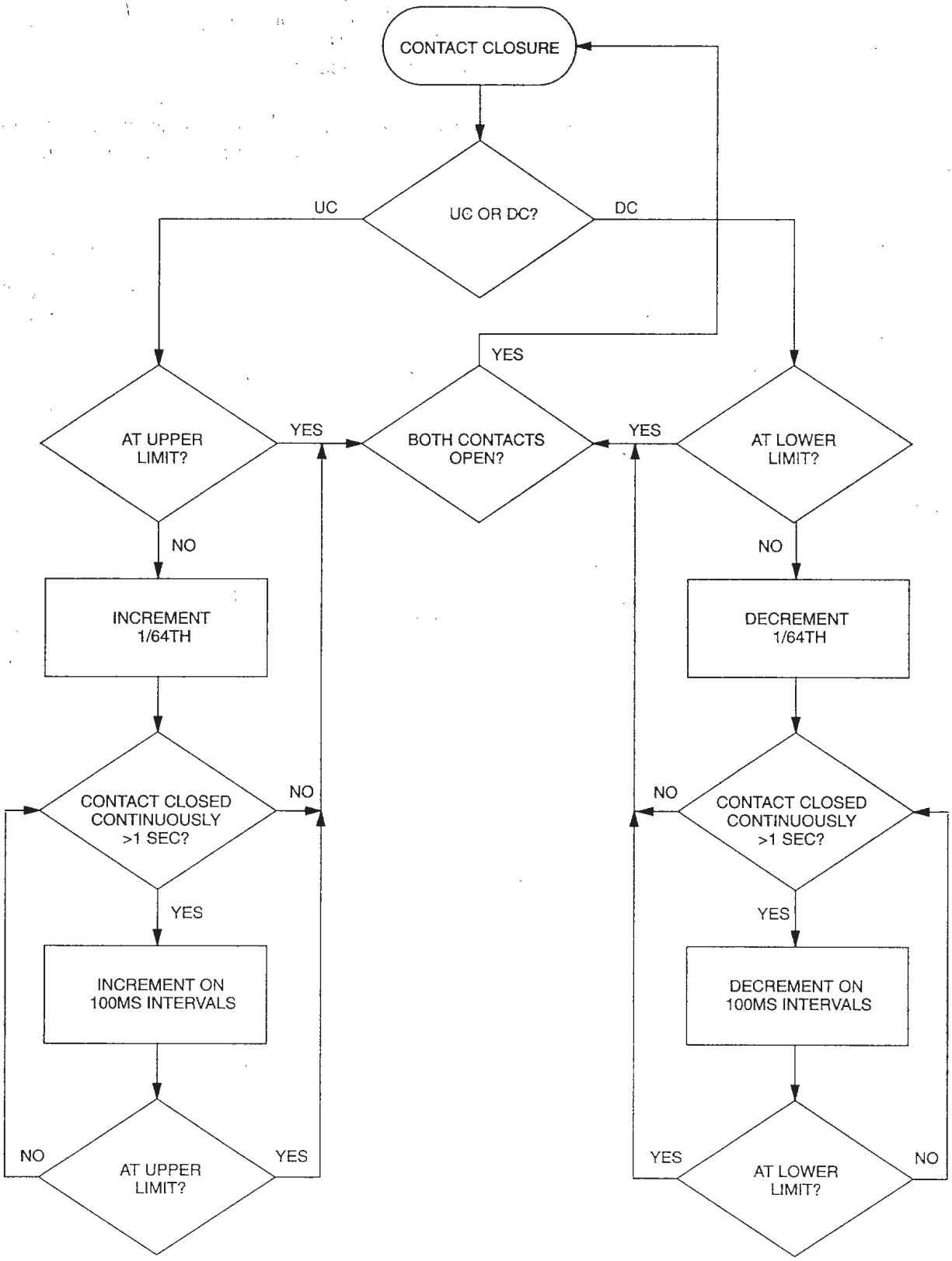
Changes or storage to the EEPROM memory cells must allow for a 2 second delay to guarantee that updates will occur. The EEPROM memory cells are specified to accept greater that 50,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the Dallastat will still function properly while power is applied. However, on power–up the device's wiper position will be that of the position last recorded before memory cell wear out.

FLOWCHART: ONE BUTTON OPERATION AND ELECTRICAL CONTROL Figure 3



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 second ± 15%

FLOWCHART: TWO BUTTON OPERATION Figure 4



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 second ± 15%

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V –0.5V + 8.0V
Operating Temperature	-20°C to 70°C commercial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	+V	-V + 2.7		-V + 8.0	V	
- Supply Voltage	-V	+V - 8.0		+V - 2.7	V	
Rheostat Inputs	R_H,R_W,R_L	-V - 0.5		+V + 0.5	V	
Logic Input 1	V_{IH}	+2.4			V	1, 2, 10
Logic Input 0	V_{IL}			+0.8	V	1, 2, 10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; -V to +V = 2.7V to 8.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+, - Supply Current	I_{CC1}		1	2	mA	3
Supply Current, Idle State At 3.3V At 8.0V	I_{CC2}			 2 10	µA	9
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	5
Rheostat Current	I_H, I_L			1	mA	5

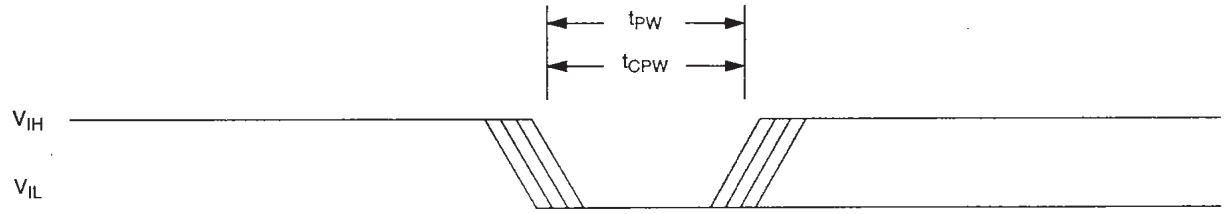
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; -V to+V = 2.7V to 8.0V)

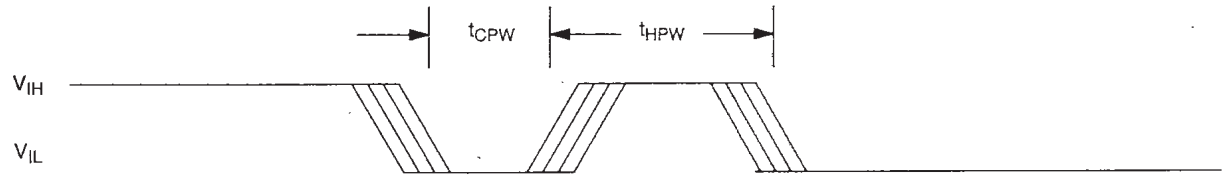
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width (D–input)	t_{PW}	1		DC	µs	1, 7, 8
Contact Pulse Width (UC, DC inputs)	t_{CPW}	1		DC	ms	1, 7, 8
Capacitance	C_{IN}		5	10	pF	6
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	1, 7, 8
Continuous Input Pulse	t_{CCP}	1		DC	s	1, 7, 8

TIMING DIAGRAMS Figure 5

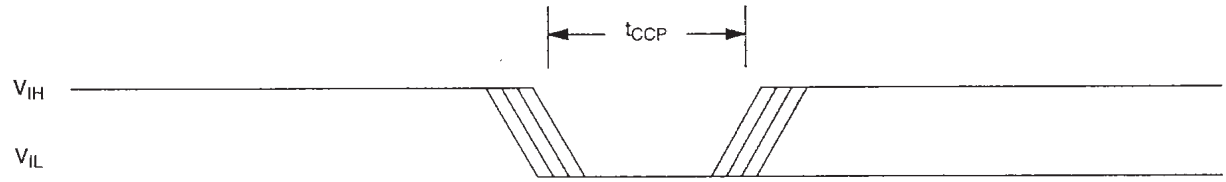
(A) SINGLE PULSE INPUTS



(B) REPETITIVE PULSE INPUTS



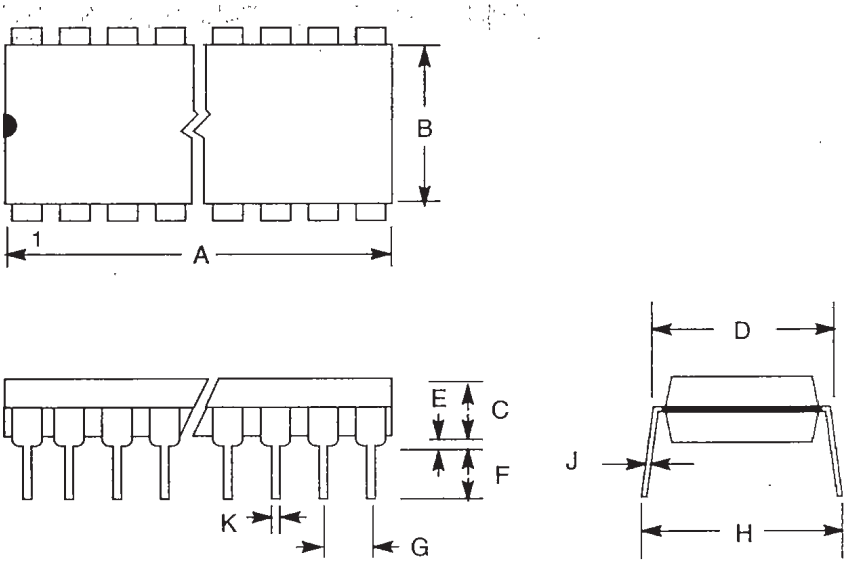
(C) CONTINUOUS PULSE INPUTS



NOTES:

1. All inputs; UC, DC, and D are internally pulled up with a resistance of 100KΩ.
2. Input logic levels are referenced to -V.
3. I_{CC} is the internal current that flows between -V and +V.
4. Input leakage applies to contact inputs UC and DC and digital input (D).
5. Wiper current and rheostat currents are the maximum current which can flow in the resistive elements.
6. Capacitance values apply at 25°C.
7. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UC, DC or D input is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UC, DC, and/or D is released to V_{IH}.
8. Repetitive pulsed inputs on UC, DC, or D will be recognized as long as the pulse repetition occurs within 1 second of each other. Pulses occurring faster than 1 ms apart may not be recognized as individual inputs but can be interpreted a constant input. Tolerances for pulse timing ±15% on minimum inputs.
9. Idle state supply current is measured with no pushbutton pressed and with the wiper R_W tied to a CMOS load.
10. For +V referenced to –V=5V.

8– TO 28–PIN DIP (300 MIL)



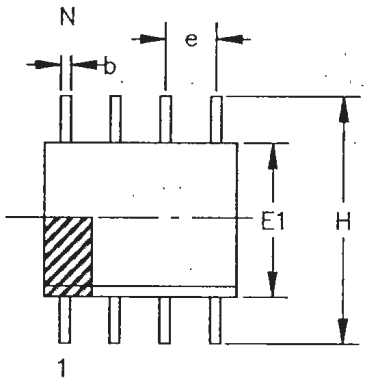
Includes:

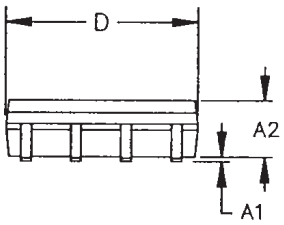
DS1000	DS1228	DS1640
DS1000M	DS1229	DS1651
DS100O–IND	DS1231	DS1652
DS1000M–IND	DS1232	DS1652B
DS1003	DS1232LP	DS1653
DS1003M	DS1234	DS1666
DS1004M	DS1236	DS1667
DS1005	DS1236A	DS1669
DS1005M	DS1237	DS1705
DS1007	DS1238	DS1706
DS1010	DS1238A	DS1707
DS1012M	DS1239	DS1708
DS1013	DS1267	DS1800
DS1013M	DS1275	DS1802
DS1020	DS1291	DS1803
DS1033M	DS1293	DS1804
DS1035M	DS1336	DS1806
DS1040M	DS1620	DS1832
DS1044	DS1621	DS1834
DS1045	DS1623	DS1866
DS1210	DS1624	DS1867
DS1211	DS1625	DS1868
DS1221	DS1632	DS1869

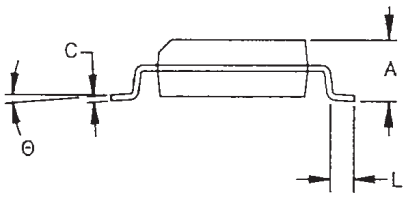
PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.360 9.14	0.400 10.16	0.480 12.19	0.520 13.21	0.740 18.80	0.780 19.81	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60	0.240 6.10	0.260 6.60	0.240 6.10	0.260 6.60	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26	0.300 7.62	0.325 8.26	0.300 7.62	0.325 8.26	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02	0.015 0.38	0.040 1.02	0.015 0.38	0.040 1.02	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56	0.110 2.79	0.130 3.30	0.120 3.O4	0.140 3.56	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40	0.320 8.13	0.370 9.40	0.320 8.13	0.370 9.40	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53	0.015 0.38	0.021 0.53

Continued on following page.

8–PIN SOIC (208 MIL)







Includes:
DS1620S
DS1623S
DS1624S
DS1625S
DS1651S
DS1652S
DS1669S
DS1821S
DS1869
DS2404

PKG	8-PIN	
DIM	MIN	MAX
A IN. MM	0.072 1.83	0.084 2.13
A1 IN. MM	0.004 0.102	0.010 0.25
A2 IN. MM	0.070 1.78	0.080 2.03
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.006 0.15	0.010 0.25
D IN. MM	0.203 5.16	0.215 5.46
e IN MM	0.050 BSC 1.27 BSC	
E1 IN MM	0.203 5.16	0.213 5.41
H IN. MM	0.302 7.67	0.318 8.07
L IN. MM	0.019 0.48	0.030 0.76
Θ	0°	8°