Princeton Technology Corp.
Tel: 886-2-29162151
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

Enhanced Digital Echo IC PT2395

DESCRIPTION

PT2395 is a silicon gate CMOS-processed digital echo IC functionally compatible with M50195P. Input signal to PT2395 is converted to digital signal with A-D conversion then stored in the memory (DRAM) chip. After a certain delay time, digital signal is read out from the memory chip and then converted back into analog signal using the D-A conversion. A low cost echo system may thus be achieved with PT2395's A-D converter, D-A converter, incorporating ADM algorithm, while maintaining lower noise, lower distortion, higher S/N ratio as compared to the conventional BBD (Bucket Brigate Device). PT2395 further features enhanced functions such as continuous delay time with external VR (Variable Resistor), 256 K DRAM support for longer delay time (Extended Delay Mode, up to 800 ms at 4 MHz Clock) as compared to M50195P. Moreover, the distortion and the S/N Ratio are further improved.

FEATURES

- CMOS Technology
- Available in 40-pin PDIP Package (600 mil)
- Low Noise, Low Distortion Echo System
- 3-Level Delay Time Selectable, with Indicator Output
- On-chip RC Oscillator for Continuous Delay Time
- 64K/256K DRAM chip support
- Extended Delay Mode up to 800 ms Delay Time (without VR)
- Create fascinating echo effect with time delay

APPLICATIONS

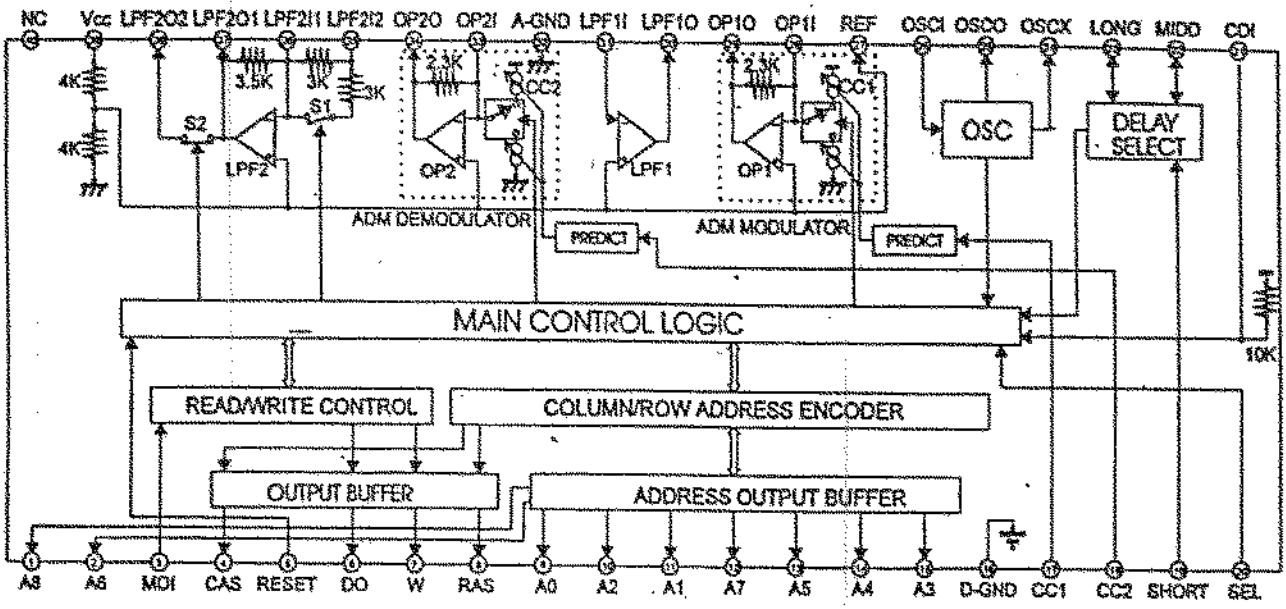
- KARAOKE
- Radio Set
- Video Disc Player
- Electronic Musical Instrument

Tel: 886-2-29162151
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

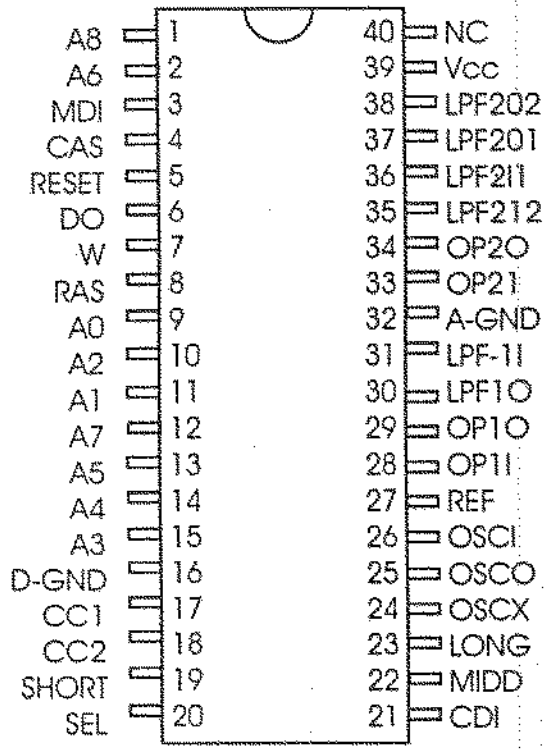
Enhanced Digital Echo IC

PT2395

BLOCK DIAGRAM



PIN CONFIGURATION



PT2395

INTERNAL BLOCK DESCRIPTION

REF: Reference Voltage Generation Circuit

Analog Circuitry that generate 1/2 Vcc Reference Voltage for Bias Voltage of OP Amplifiers.

LPF1, LPF2: Low Pass Filter

LPF1 filters undesirable high frequency from the input signal to avoid malfunction in the A-D conversion.

LPF2 filters away sampling frequency, ripple and noise from the D-A Output Signal.

OP1, CC1: ADM Modulator

OP Amplifier (OP1) and Current Control Loop (CC1) plus External Comparator construct an ADM Modulator to digitize input signal with Adaptive Delta Modulation Method.

OP2, CC2: ADM Demodulator

OP Amplifier (OP2) and Current Control Loop (CC2) construct an ADM Demodulator to convert digitized signal back to analog signal.

Two Delta Forecaster:

To predict the most suitable delta adjustment for best distortion and S/N Ratio.

Oscillator:

Generates the master clock for logic circuit, with external crystal. Standard Clock Frequency equals to 4 MHz. An RC Oscillator may also be constructed with a 30 pF capacitor, a 470 Ohms Resistor, a 1 K Ohm Resistor and a 5 K Ohm VR to generate approximately 2.5 to 6 MHz Clock Frequency.

Delay Time Selecting Circuitry:

High Level asserted on either Pin 19, 22, 23 selects SHORT (100 ms), MIDD (150 ms), LONG (200 ms) Delay Time respectively. ($MHz, 64 K DRAM)

S1: Gain and Low Frequency Response Switch

When SHORT Delay Time is selected, S1 is ON. In this case, the output gain is 6 dB higher than output gain generated when MIDD or Long is selected. An external capacitor should be connected to Pin 32. The frequency response below 240 Hz is cutoff when SHORT is selected. When MIDD or LONG is selected the frequency response below 120 Hz is cutoff. Please note that 0.47 μF capacitor is connected between Pin 34 and Pin 35).

S2: Feedback Gain Switch

When LONG Delay Time is selected, S2 is OFF. When SHORT or MIDD Delay Time is selected, S2 is ON so that the feedback gain is higher than that when LONG is selected.

Main Control Logic:

Combined Control Circuit for ADM Modulator and Demodulator, Delay Time and Memory Control.

Read/Write Logic:

Memory Chip Read/Write Control Logic

Column, Row Address Encoder:

Memory Chip Column/Row Address Generation

Output Buffer and Address Buffer:

External Memory Chip Driver. (Maximum 10pF loading)

SEL: 64 K/256 K DRAM Chip Select

To enter Extended Delay Mode, assert High Level and use 256 K DRAM for longer delay time. Open if 64 K DRAM (or 256 K DRAM used as 64 K DRAM) is used.

PIN DESCRIPTION

Pin No.	Pin Name	Description	Usage	Standard Output Voltage
1	A8	Memory Chip Address A8 Output	Connect to A8 Address Input of 256 K DRAM	5Vp-o
2	A6	Memory Chip Address A6 Output	Connect to A6 Address Input of Memory Chip	5Vp-o
3	MDI	Memory Data Input	Connect to Memory Data Output	-
4	CAS	Column Address Strobe Output	Connect to Memory Chip Column Address Strobe Input Pin	5Vp-o
5	RESET	Reset Input	Connect External R, C for Low Level Reset when Power ON	-
6	DO	Data Output	Connect to Memory Chip Data Input Pin	5Vp-o
7	W	Write Control Output	Connect to Memory Chip Write Control Input	
8	RAS	Row Address Strobe Output	Connect to Memory Chip Row Address Strobe Input	
9	A0	Address 0 Output	Connect to Memory Chip A0 Address Input	
10	A2	Address 2 Output	Connect to Memory Chip A2 Address Input	
11	A1	Address 1 Output	Connect to Memory Chip A1 Input	
12	A7	Address 7 Output	Connect to Memory Chip A7 Input	
13	A5	Address 5 Output	Connect to Memory Chip A5 Input	
14	A4	Address 4 Output	Connect to Memory Chip A5 Input	
15	A3	Address 3 Output	Connect to Memory Chip A3 Input	
16	D-GND	Digital Ground	Connect together with A-GND	0V
17	CC1	Current Control 1	Connect External Capacitor	0.7V (When no signal)
18	CC2	Current Control 2	Connect External Capacitor	
19	SHORT	SHORT Delay Time Select	When "High Level" is asserted, the Delay Time , Td = 100 ms. Standard Indicator Output Current = 5mA	5V (SHORT) 0V (MIDD or LONG)

Enhanced Digital Echo IC

PT2395

Pin No.	Pin Name	Description	Usage	Standard Output Voltage
20	SEL	Select 256 K DRAM Chip	Connect to "High" when 256 K DRAM is used in Extended Delay Mode	-
21	CDI	Comparator Data Input	Connect to Comparator Data Output	-
22	MIDD	MIDD Delay Time Select	When "High Level" is asserted, the Delay Time Td = 150 ms. Standard Indicator Output Current = 5mA	5V (MIDD) 0V (SHORT or LONG)
23	LONG	LONG Delay Time Select	When "HIGH Level" is asserted, the Delay Time Td = 200 ms. Standard Indicator Output Current = 5 mA	5V (LONG) 0V (SHORT or MIDD)
24	OSCX	Extra Oscillator Output	Construct RC Oscillator with OSCI and OSCO. (*Refer to Application Circuit*)	-
25	OSCO	Oscillator Output	Connect 4 MHz Crystal. Open when using External Clock Source	5Vp-o
26	OSCI	Oscillator Input	Connect 4 MHz Crystal or External Clock Source	5Vp-o
27	REF	Reference Voltage	≅ 1/2 Vcc	2.5V
28	OP1I	OP Amplifier 1 Input	Construct Miller Integrator with External Capacitor	2.5V
29	OP1O	OP Amplifier 1 Output		2.5V
30	LPF1O	Low-Pass Filter 1 Output	Construct 2nd Order Low-Pass Filter with External R,C	2.5V
31	LPF1I	Low-Pass Filter 1 Input		2.5V
32	A-GND	Analog Ground	Construct together with D-GND	0V
33	OP2I	OP Amplifier 2 Input	Construct Miller Integrator with External Capacitor	2.5V
34	OP2O	OP Amplifier 2 Output		2.5V
35	LPF2I2	Low-Pass Filter 2 Input 2	Connect External Capacitor between Pin 34 and Pin 35 to construct a Low-Pass Filter with cutoff frequency f_{c2}=240 Hz (when SHORT) and f_{c2}=120 Hz (when MIDD, LONG)	2.5V
36	LPF2I1	Low-Pass Filter 2 Input 1	Connect External Capacitor between Pin 36 and Pin 37 to construct a Low-Pass Filter with cutoff frequency f_{c3} = 5.7 KHz	2.5V
37	LPF2O1	Low-Pass Filter 2 Output 1		2.5V
38	LPF2O2	Low-Pass Filter 2 Output 2	Damping then Feedback to Analog Input Signal	2.5V
39	Vcc	Power Supply Voltage	DC 4 ~ 5.5V	-
40	NC	No Connection	-	-

FUNCTIONAL DESCRIPTION

Input audio signal is first fed into the LPF1 to filter away undesirable high frequency energy. Output of the LPF1 is then converted into digital signal via the built-in ADM modulator and external comparator. Such ADM digital signal is called 1 bit digitized signal. The digital signal is fed to Pin 21 (CDI) and flows into the Main Control Logic. The appropriate address of the digitized signal stored into external memory chip is selected by the Main Control Logic. The Main Control Logic also addresses the memory chip to retrieve the contents stored for a given period of time. The retrieved contents are fed to the ADM demodulator and are converted back to analog signal.

ADM Demodulator are of the same structure as the ADM Modulator. The demodulated signal is further fed to LPF2 to filter away undesirable high frequency energy and sampling frequency. The signal is then outputted from Pin 37. As described above, the input signal is delayed for a certain period of time and then fed back to the input signal. In this way, the echo effect is then achieved.

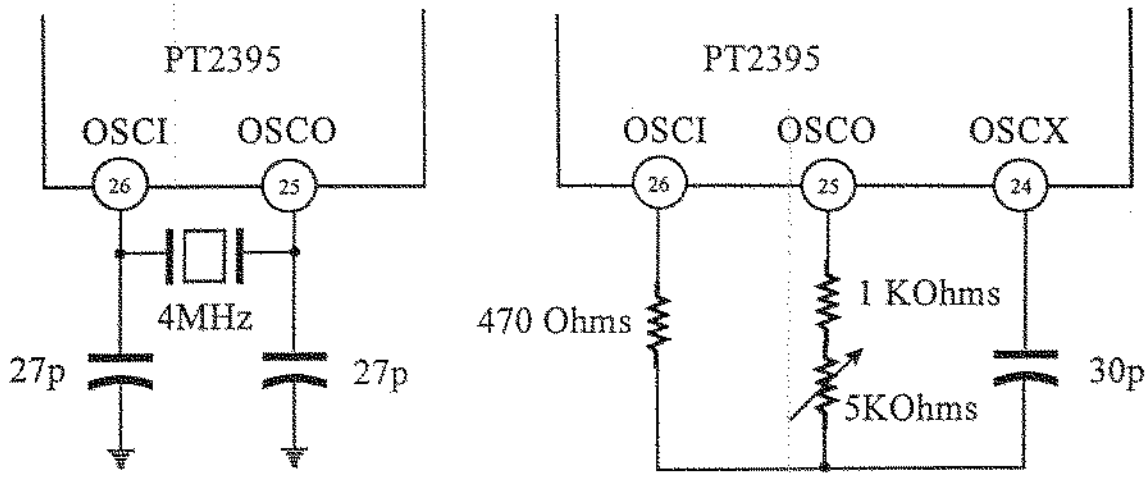
PT2395 digitizes the input signal and stores it into the memory chip. After some delay time, PT2395 retrieves the digitized signal and converts it back to analog signal. In this way, a low noise and low distortion delay signal is derived by means of digital delay. A low cost echo system is thus achieved with this 1 bit ADM method.

DELAY TIME SELECT GUIDE

SHORT	MIDD	LONG	SEL	4 MHz Clock			Extended Delay Time
				Sampling Rate	Delay Time	DRAM Chip	
	Low	Low	Open/Low	500 KHz	98.3ms	64K/256K	No
Low			Open/Low	250 KHz	147.5ms	64K/256K	No
Low	Low		Open/Low	250 KHz	196.6ms	64K/256K	No
	Low	Low	High	500 KHz	393.2ms	256K	Yes
Low			High	250 KHz	590ms	256K	Yes
Low	Low	Low	High	250 KHz	786.4ms	256K	Yes

OSCILLATOR

Either a 4 MHz Crystal Oscillator or RC Oscillator may be used with PT2395. With 4 MHz Crystal Oscillator, fixed echo delay time may be achieved as indicated in the Delay Time Select Table. If continuous delay time adjustment is desired, an RC oscillator with VR may be used. The following diagrams indicate how both oscillators may be built with PT2395.



64 K / 256 K DRAM SELECT

Either 64 K (4164) or 256 (41256) DRAM may be used with PT2395 as Memory Chip. When 256 K DRAM is used, the Extended Delay Mode may be selected by connecting SEL (Pin 20) to Vcc. Long Echo Delay may be achieved in the Extended Delay Mode.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
Vcc	Power Supply Voltage	7	V
Icc	Supply Current	70	mA
Pd	Internal Power Dissipation	1100	mW
Topr	Ambient Temperature During Operation	-20 to +75	oC
Tstg	Storage Temperature	-40 to +125	oC

ELECTRICAL CHARACTERISTICS

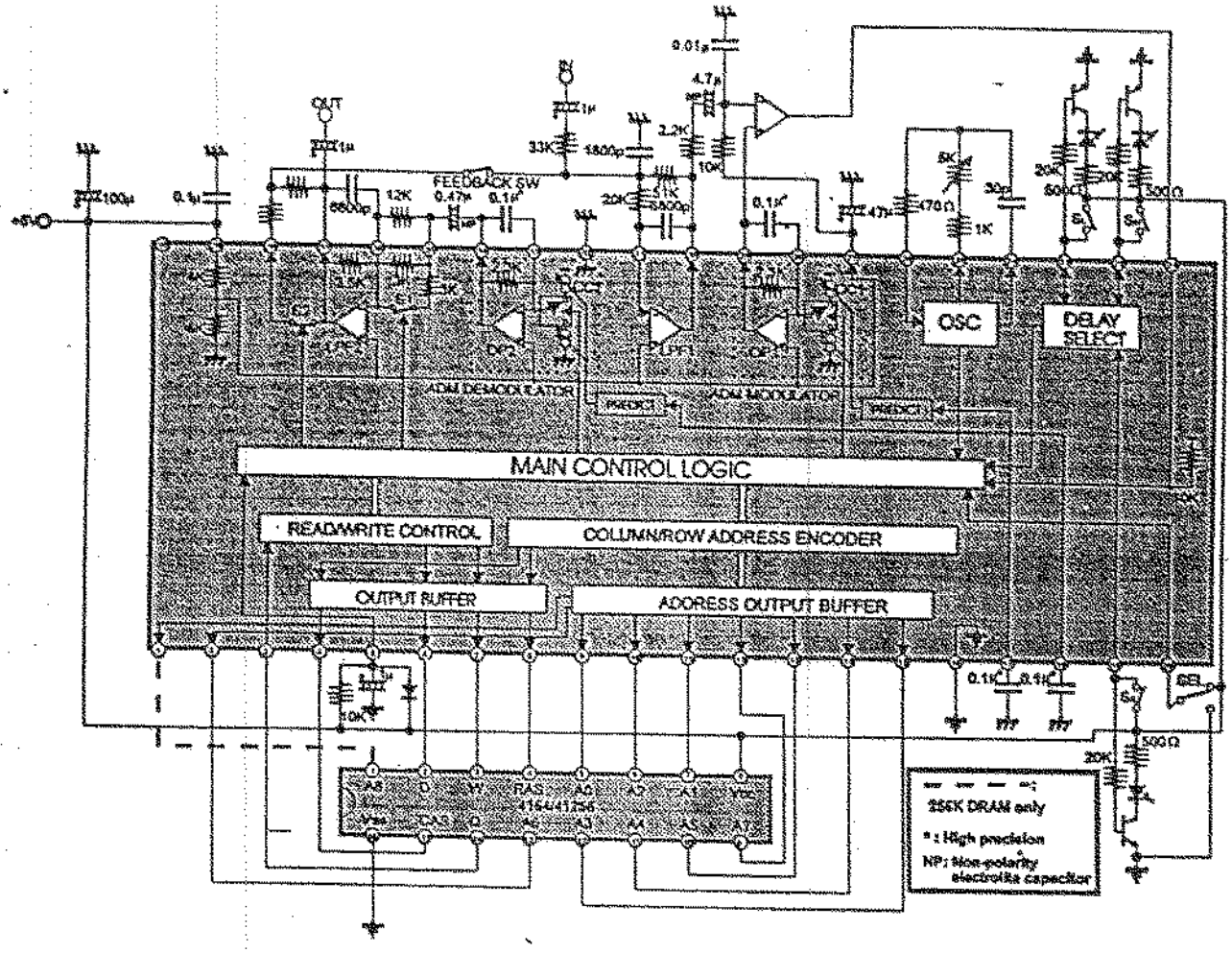
(Vcc=5V, f-1, Vi=100m Vrms, fck=4MHz, R_L=10 K Ohms, Ta=25°C)

Symbol	Parameter	Condition		Min.	Nom.	Max.	Unit
Icco	Operating Current	No Input			15		mA
GVS		SHORT asserted			11		dB
GVM		MIDD asserted			5		dB
GVL		LONG asserted			5		dB
Tds	Delay Time	SHORT asserted			98.3		msec
TdM		MIDD asserted			147.5		msec
TdL		LONG asserted			196.6		msec
Vomax	Maximum Output Voltage	SHORT asserted	THD=3%		1.7		Vrms
		MIDD or LONG asserted			1.1		
THD	Output Distortion	Short asserted, Vo=1 vrms			0.4		%
No	Output S/N Ratio	Short asserted	Rg=50 DIN-AUDIO		-89		dBV
		MIDD or LONG asserted			-93		
Δ VRR	Supply Voltage Rejection Ratio	ΔVcc=-20dBV, 100Hz			-40		dB

DC CHARACTERISTICS

Symbol	Parameter	Applied Pin & Test Condition	Rating			Unit
			Min.	Nom.	Max.	
Vcc	Supply Voltage		4	5	5.5	V
fck	Clock Frequency		2.5	4	6	MHz
V_{IH}	"H" Level Input Voltage	MIDI, RESET, CDI. SHORT, MIDD. LONG, SEL	0.8Vcc	· Vcc	Vcc	V

APPLICATION CIRCUIT

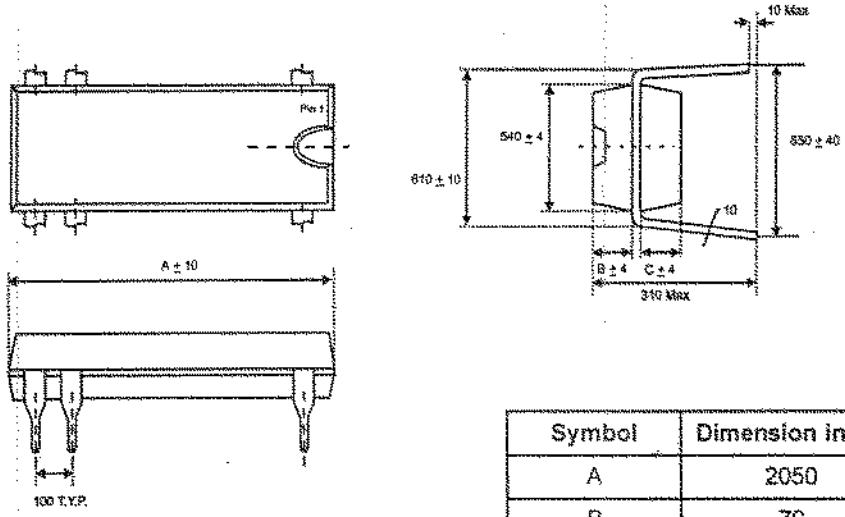


ORDER INFORMATION

Valid Part Number	Package Type
PT2395	40 PDIP (600 mil)

PACKAGE INFORMATION

40-Pin, DIP Package (600 mil)



Symbol	Dimension in Mil
A	2050
B	70
C	70