MN3005

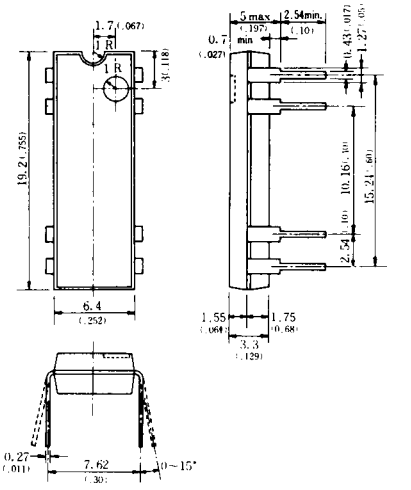
4096-STAGE LONG DELAY BBD

■ General description

The MN3005 is a world's first 4096-stage long delay BBD, 8 times longer than 512-stage BBD manufactured by using a P-channel low noise silicon gate process.

Long signal delay time 205ms can be obtained at clock frequency 10KHz. S/N is 75dB. S/N has been improved by more than 20dB in comparting with 8-connected 512-stage BBD's. The MN3005 is suitably used for reverberation and echo effects in electronic musical instruments such as electronic organ, guitar amplifier and music synthesizer which need long delay time.

Unit: mm (inch)



Special 8-Lead Dual-In-Line Plastic Package

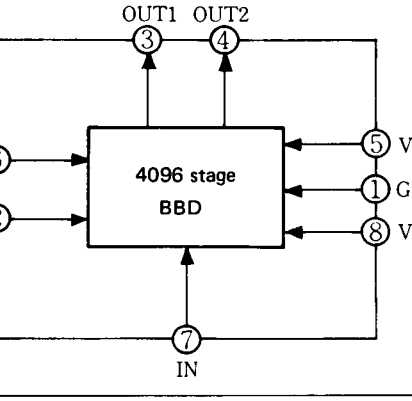
■ Features

- 1 chip 4096 stage and wide range of variable delay times: 20.48 ~ 204.8ms.
- High S/N in spite of multi-stage and wide dynamic range: S/N ≃ 75dB typ.
- No insertion loss since the loss occuring in the signal transfer is corrected by the MOS capacity of input and output. L_i = 0dB.
- High integration and high reliability by using P channel low noise silicon gate process.
- Special 8 lead dual-in-line plastic package.

■ Applications

- Reverberation and echo effects in echo microphone and stereo equipment.
- Chorus effect in electronic musical instruments.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication systems, etc.

■ Block Diagram



■ Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD} + 1	V
Signal Delay Time	t_D	20.48~204.8	ms
Total Harmonic Distortion	THD	1	%
Signal to Noise Ratio	S/N	75	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18~+0.3	V
Output Voltage	V_O	−18~+0.3	V
Operating Temperature	Topr	−20~+60	℃
Storage Temperature	Tstg	−55~+125	℃

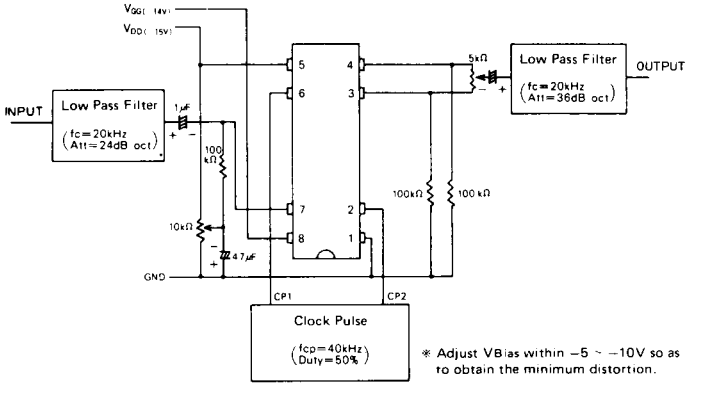
■ Operating Conditions (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−14	−15	−16	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−1	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Input Capacitance	C_{CP}				2800	pF
Clock Frequency	f_{CP}		10		100	kHz
Clock Pulse Width *2	t_{cpw}	Test Circuit			0.5T※2	
Clock Rise Time *2	t_{cpr}	Test Circuit			500	ns
Clock Fall Time *2	t_{cpf}	Test Circuit			500	ns
Clock Cross Point	V_X		0		−3	V
Input DC Bias Voltage	V_{Bias}		−5		−10	V

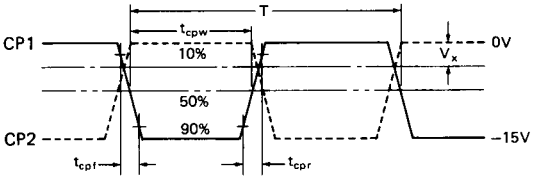
■ Electrical Characteristics (Ta = 25°C, V_{DD} = V_{CPL} = −15V, V_{CPH} = 0V, V_{GG} = −14V, R_L = 100kΩ)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		20.48		204.8	ms
Input Signal Frequency	f_i	f_{CP} = 40kHz, V_i = 1.0Vrms, Output Attenuation ≦ 3dB (0dB at f_i = 1kHz)	10			kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i = 1 kHz, THD=2.5%	1.0			Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i = 1 kHz, V_i =1.0Vrms	−4	0	4	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i = 1 kHz, V_i =0.78Vrms		1	2.5	%
Noise Voltage	V_{no}	f_{cp} = 100kHz Weighted by "A" curve			0.4	mVrms
Signal to Noise Ratio	S/N			75		dB

■ Test Circuit

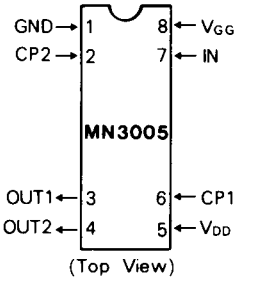


*1 Clock Pulse Waveforms

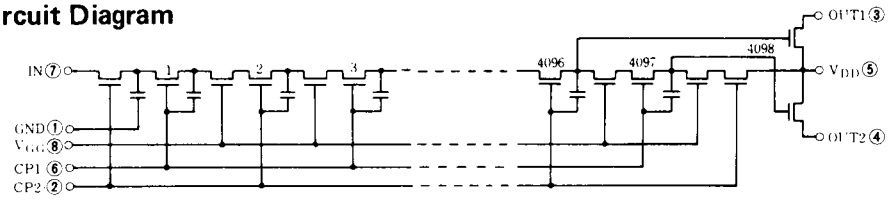


*2 T = 1/fcp

■ Terminal Assignments

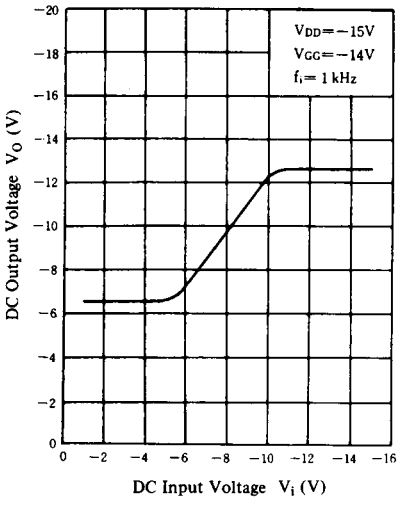


■ Circuit Diagram

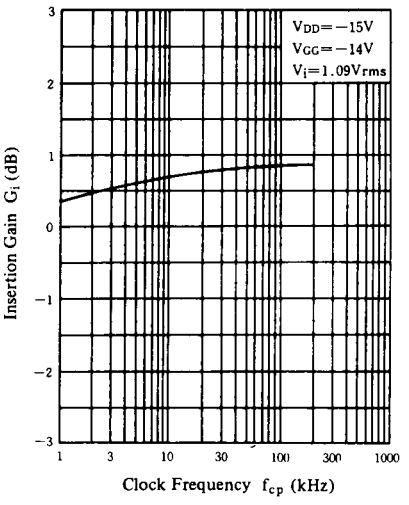


■ Typical Electrical Characteristic Curves

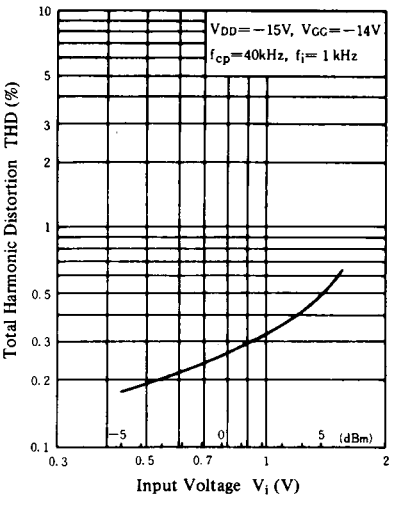
V_O—V_I



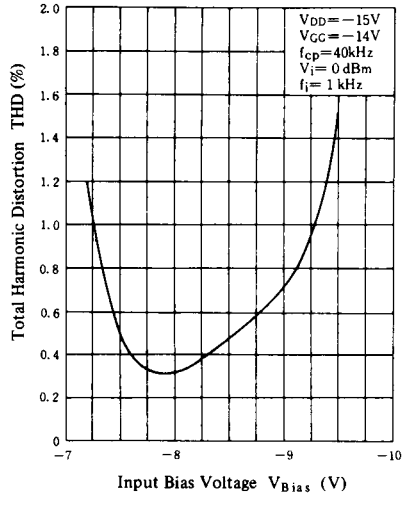
G_i—fcp



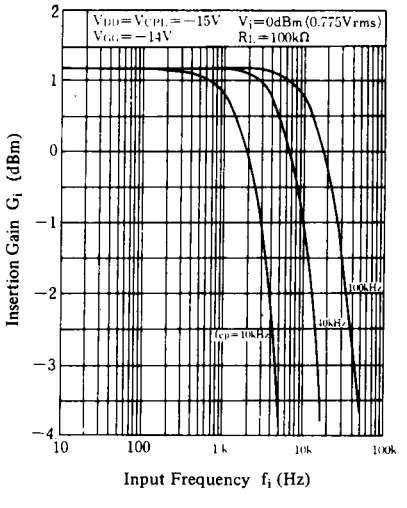
THD—V_i



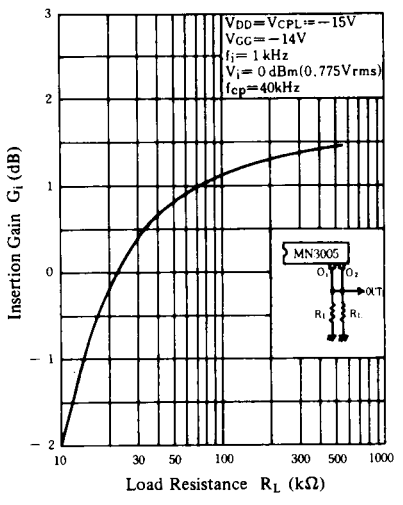
THD—V_{Bias}



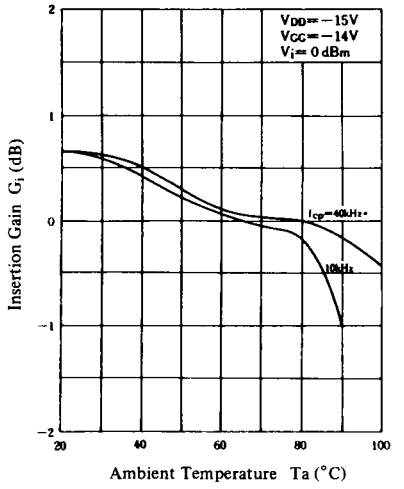
G_i—f_i



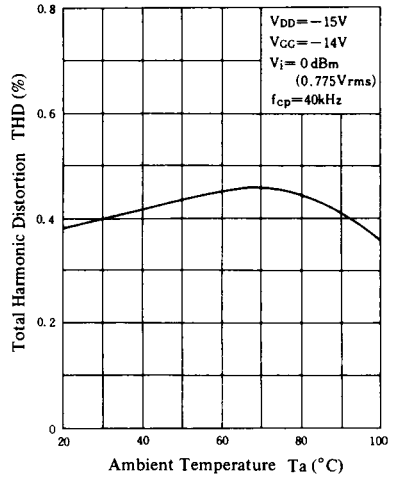
G_i—R_L



G_i—Ta

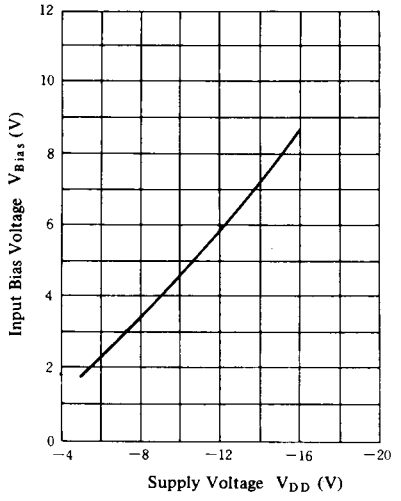


THD—Ta

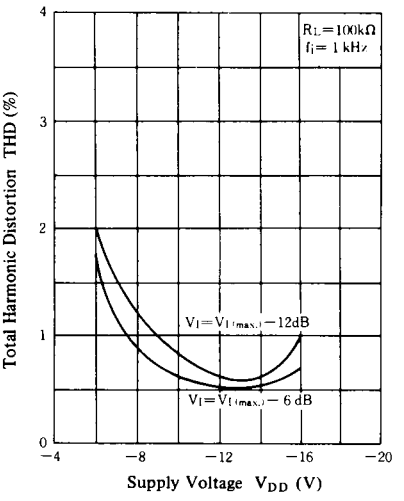


■ Supply Voltage Characteristics

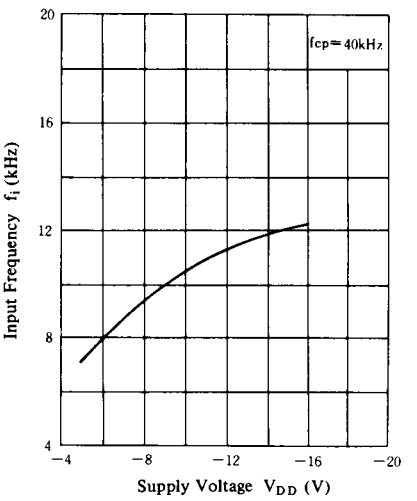
V_{Bias}—V_{DD}



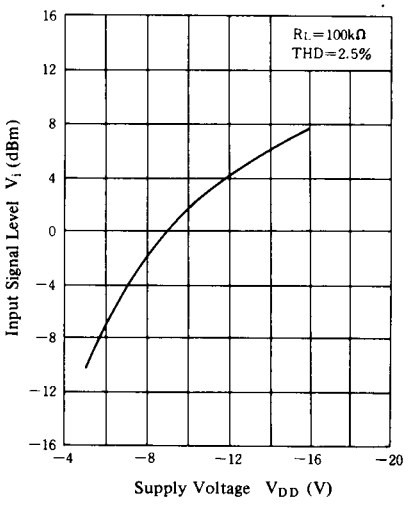
THD—V_{DD}



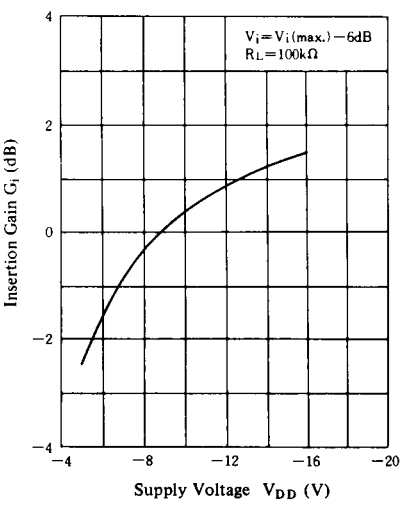
f_i—V_{DD}



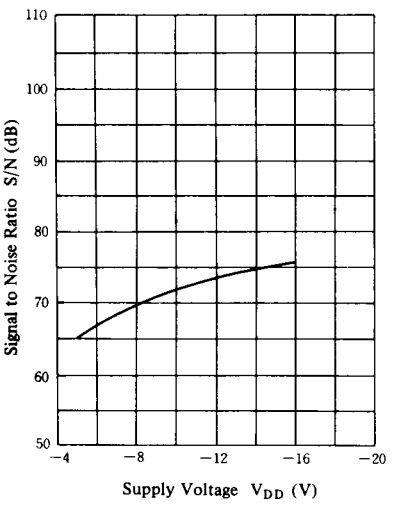
V_i—V_{DD}



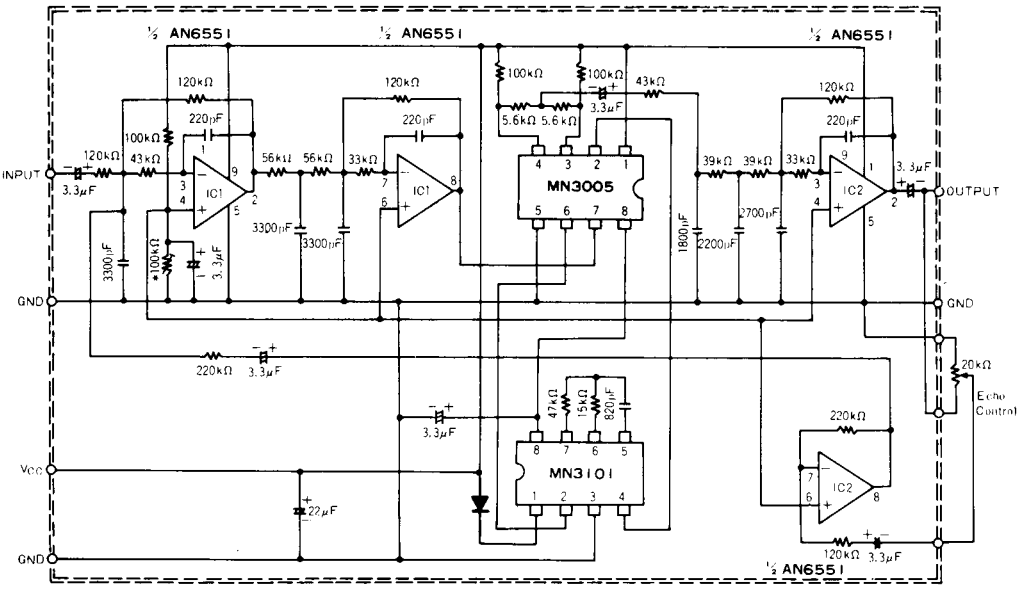
G_i—V_{DD}



S/N—V_{DD}



■ Application Circuit



Reverberation Effect Generation Circuit (Signal Delay Over 100msec.)

■ Pattern Drawing of the Printed Circuit Board (Real size)